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Total Harmonic Distortion Comparison between Sinusoidal PWM Inverter and Multilevel Inverter in Solar Panel

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Abstract

This research compared the performance of PWM (*Pulse Width Modulation*) *inverter and multilevel inverter in terms of their output voltage and current total harmonic distortion* (*THD*). *The inverters were designed to have the output voltage of 220 V at 50 Hz. The input voltage for both inverters are 400 VDC. For PWM inverter, the PWM technique utilized was sinusoidal PWM* (*SPWM*) *and for multilevel converter, the number of voltage level is five with diode-clamped topology. The study included circuit implementation, analysis, and THD calculation, all of which were carried out through simulation using PSpice software. In controlling the SPWM inverter output, the adjusted parameters included amplitude modulation ratio, frequency modulation ratio, and filter components' parameters. On the other hand, the firing angles of the switching components were designated as controlling parameters in multilevel inverter. From the study, it was found that the best THD values of the designed SPWM inverter are 4.2%* (*voltage*) *and 1.7%* (*current*)*, while those of multilevel inverter are 27% and 11%, for voltage and current, respectively. Thus, it can be concluded that SPWM inverter is better than 5-level inverter for the application in solar panel due to its lower THD. In our study, 5-level inverter did not satisfy the THD requirement specified in IEEE 512-1992, i.e. 5%.*

Keywords: *THD; PWM Inverter; Multilevel Inverter; Inverter Simulation*

1. Introduction

With high penetration of renewable energy sources in power grid, the use of power converters becomes indispensable. Attention is given when renewable energy is extracted through DC-generating equipment, e.g. solar panel. Strictly speaking, solar panel cannot be directly connected to existing AC power grid. Instead, it should be connected through what-so-called 'inverter'. Power inverters deliver and control power generated by solar panel by converting its DC voltage to AC voltage. Through inverter, a single solar panel can be connected to existing AC grid. Alternatively, several solar panel can team up to form a DC grid and then connected to AC grid through high-power inverter.

Challenge often faced when employing switch-mode power inverter is the inverter output harmonics. The presence of harmonics distorts the inverter output, such that it is not in the form of pure sinusoidal. The severity of output harmonics is usually expressed as 'total harmonic distortion' (THD). THD is observed at both inverter output voltage and current. As per IEEE standard, the maximum THD allowed is ±5% [1].

THD reduction can be carried out by using inverter circuit manipulation and by using external control. Circuit manipulation is realized by improving inverter topology, while external control is by modifying gate signal injected to switching components, i.e. MOSFET. One of improved inverter topology is the multilevel inverter. Multilevel inverter topology possess several advantages, including the possibility of being used in high-voltage application, low switching losses, high efficiency, and low electromagnetic interference [2][3][4]. On the other hand, one of external control schemes is the use of sinusoidal pulse width modulation (SPWM). The main advantage of SPWM-controlled inverter is the ease of its output filtering because the harmonics occur on higher order [5][6][7].

In this paper, we present a simulation study to compare the performance of multilevel inverter and SPWM inverter. Comparison was made in terms of output waveform THD, for both voltage and current. The result of this study will be a strong recommendation for hardware implementation of the inverter.

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2. A Brief Review on Power Inverter

Inverter is a device aimed at converting DC voltage to AC voltage. Basic inverter topology is the H-bridge inverter, as shown in Figure 1. Depending on the arrangement of switches S_1 – S_4 on-off state, the inverter output voltage V_O will have values of $+V_{DC}$, 0, $-V_{DC}$. Switches S_1 – S_4 are realized in the circuit by using semiconductor devices having high-speed switching capability. MOSFET and IGBT are two common switching devices, especially when ultrahigh speed switching is required or preferred, for example in PWM inverter.

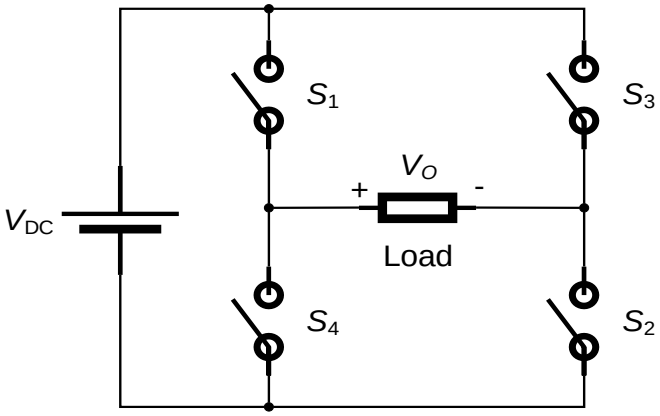


Figure 1. Basic Inverter Circuit

2.1 SPWM Inverter

PWM in inverter is a technique to control the switching operation of switches S_1 – S_4 in Figure 1 by varying MOSFET gate pulse duty cycle according to a specific pattern. This is done by comparing the instantaneous values of reference signal and carrier signal. Reference signal determines the output waveform fundamental frequency, while carrier signal (in the form of triangle) determines the switching frequency of switching components. In case the desired output of the inverter is sinusoidal waveform, reference signal should be sinusoidal. This kind of PWM is called sinusoidal PWM (SPWM). SPWM is illustrated in Figure 2.

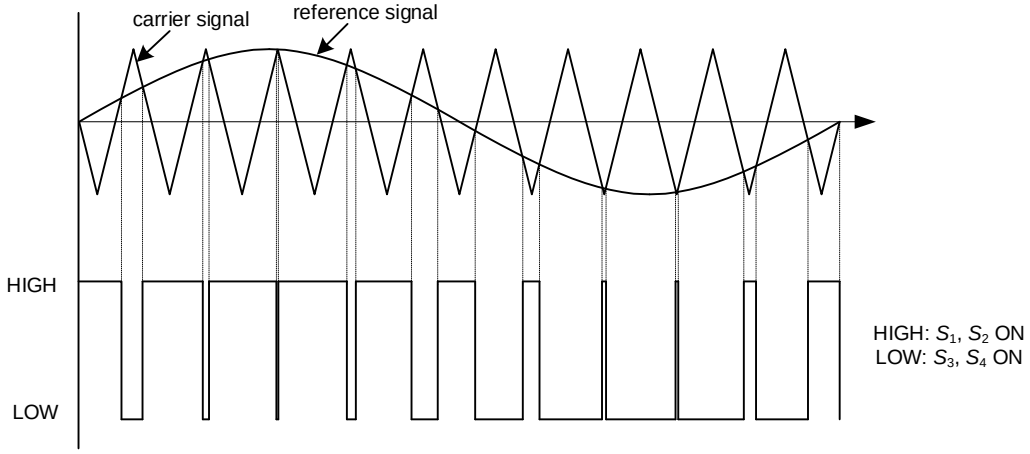


Figure 2. Reconstruction of SPWM Signal

Referring to Figure 2, there are two important parameters in controlling PWM signal, which are described as follows.

1. Amplitude modulation ratio m_a. It is the ratio between amplitude of reference signal V_{sine} and amplitude of carrier signal V_{tri}, as mathematically expressed in Equation 1.

$$m_a = \frac{V_{sine}}{V_{tri}} \quad (1)$$

The relationship between m_a and the amplitude of the inverter output fundamental component is further defined in Equation 2.

$$V_1 = m_a \times V_{DC} \quad (2)$$

where V_1 is the amplitude of the inverter output fundamental component.

2. Frequency modulation ratio m_f. It is the ratio between frequency of carrier signal f_{tri} and frequency of reference signal f_{sine}. Mathematically, it is expressed in Equation 3.

$$m_f = \frac{f_{tri}}{f_{sine}} \quad (3)$$

The original output of a SPWM inverter is indeed square-wave with varying duty cycle, as shown in Figure 2. The harmonics appears on the order of switching frequency and its multiple. A low-pass filter (LPF) was designed to further improve the SPWM performance. Higher switching frequency is preferred, since it can make filtering easier [8]. As a consequence, THD can be optimally suppressed. In this study, we employed a simple *RC* LPF, in which the values of *R* and *C* are derived from Equation 4.

$$f_c = \frac{1}{2\pi \times \frac{Z_L R}{Z_L + R} \times C} \quad (4)$$

where f_c is the cut-off frequency (Hz) and Z_L is the load impedance (Ω).

2.2 Multilevel Inverter

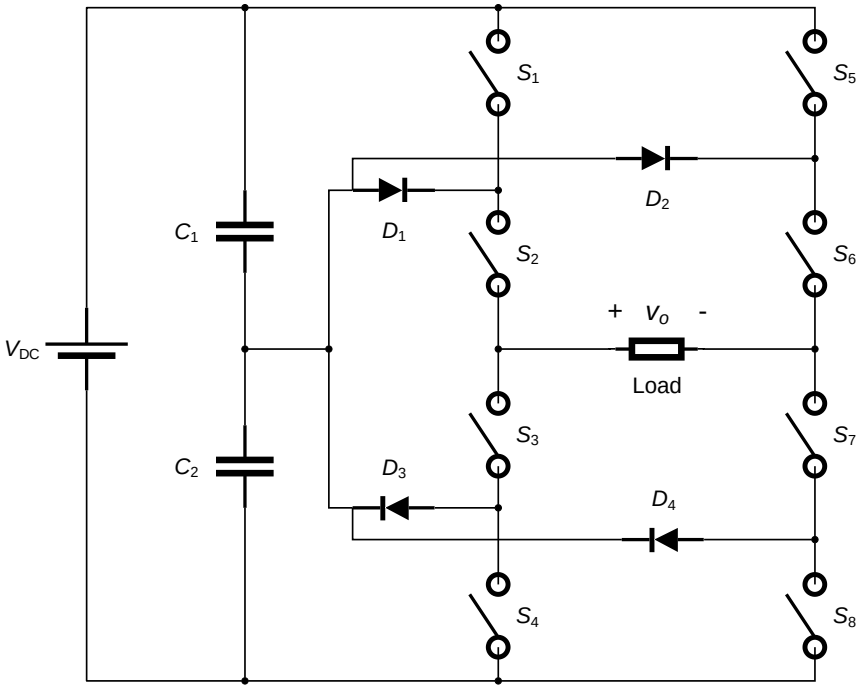
Multilevel inverter is an inverter topology formed by several individual H-bridge inverters shown in Figure 1. The output of multilevel inverter is more similar to a pure sinusoidal signal as compared with the output of original H-bridge inverter [9]. Furthermore, compared with SPWM inverter, multilevel inverter does not require very high switching frequency, hence the switching losses is reduced [10]. The need for filter can also be ignored in multilevel inverter, especially when the level is increased to a very big number. The latter, however, brings consequence of increased complexity of circuit topology. A special type of multilevel inverter is the so-called diode-clamped multilevel inverter. This type is utilized when only one DC input is available. Figure 3 shows a diode-clamped 5-level inverter topology and its associated output waveform.

Parameter that controls the output of multilevel inverter is the delay angle or firing angle α of the switching components, i.e. the angle at which the switch becomes closed. The value of α determines the output value at fundamental frequency and simultaneously controls the output THD. Quantity that relates α and the output fundamental component is called 'modulation index' and is expressed in Equation 5 [11].

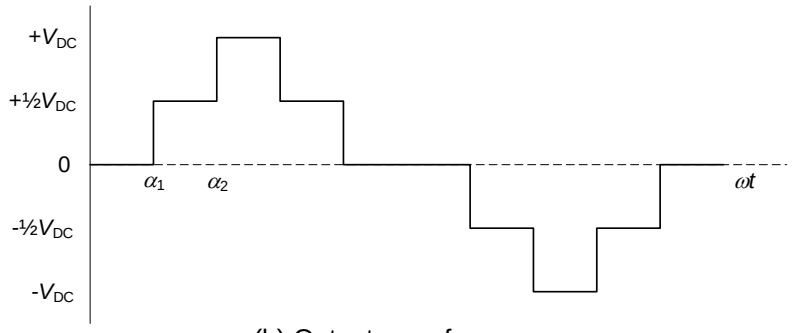
$$M_i = \frac{V_1}{s\left(4 \times \frac{V_{DC}}{\pi}\right)} = \frac{\cos\alpha_1 + \cos\alpha_2 + \ldots + \cos\alpha_s}{s} \quad (5)$$

Where M_i is the modulation index, V_1 is the magnitude of the output fundamental component, and *s* is the number of DC sources. In case of diode-clamped topology, the number of DC sources is determined by its capacitive voltage divider.

Certain harmonic order in inverter output can eliminated by proper choice of α. In 5-level inverter, there will be two values of α, denoted α_1 and α_2, as shown in Figure 3 (b). Referring to the waveform in Figure 3 (b), α_1 and α_2 are switching angles for achieving five voltage levels of $\{V_{dc}, ½V_{dc}, 0, -½V_{dc}, -V_{dc}\}$. The values of α_1 and α_2 should obey: $\alpha_1 < \alpha_2 < 90^0$. To eliminate n^{th} harmonic and its multiples, Equations 6 and 7 should be simultaneously fulfilled [11].



(a) Topology



(b) Output waveform

Figure 3. 5-Level Diode-Clamped Inverter

$$\cos n\alpha_1 + \cos n\alpha_2 = 0 \tag{6}$$

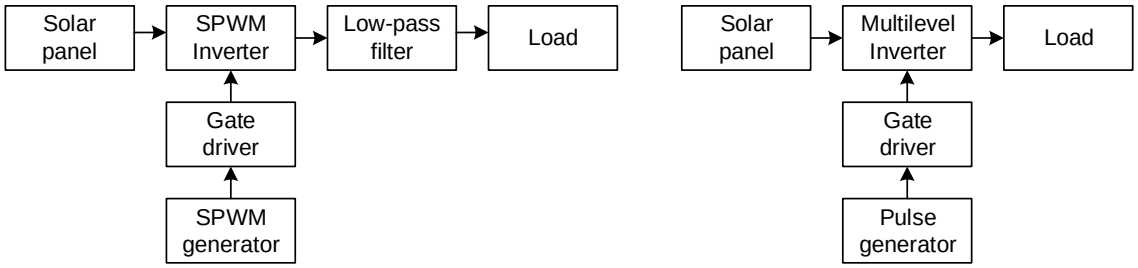
$$\cos\alpha_1 + \cos\alpha_2 = 2M_i \tag{7}$$

3. Research Method

In this section, designs of the studied inverters (SPWM and multilevel) are detailed, along with inverter specification. Figure 4 shows block diagrams of both inverter systems and the description of each component is presented as follows.

3.1 Solar Panel Modeling

The DC input to the inverters are considered as solar panel. Solar panel is formed by array of several photovoltaic (PV) cells. The model of individual PV cell is shown Figure 5 [12], [13]. It is depicted that equivalent circuit of a PV cell consists of a source current I_{ph}, a diode D, a resistance parallel with the diode R_{sh}, and a series resistance R_S. Current source I_{ph} represents the current which is proportional to solar irradiation level, while diode D represents electron and hole movement area. The diode used in this study was 1N4001. R_S is the ohmic contact level between metal and internal resistance of semiconductor material and the value was set at 0.0001 Ω in this study. Shunt resistance, R_{sh}, represents leakage current resistance to ground. A value of 10 kΩ was assigned in this study for R_{sh}.



(a) SPWM inverter (b) Multilevel inverter

Figure 4. Block Diagrams of the Studied Inverter

Figure 6 shows I-V characteristics at different solar irradiation levels. It is observed that maximum voltage level that a PV cell can produce is around 1.18 V at solar irradiation of 1000 W/m^2. We choose to give 400 V DC input to inverter; thus 340 series-arranged PV cells are needed.

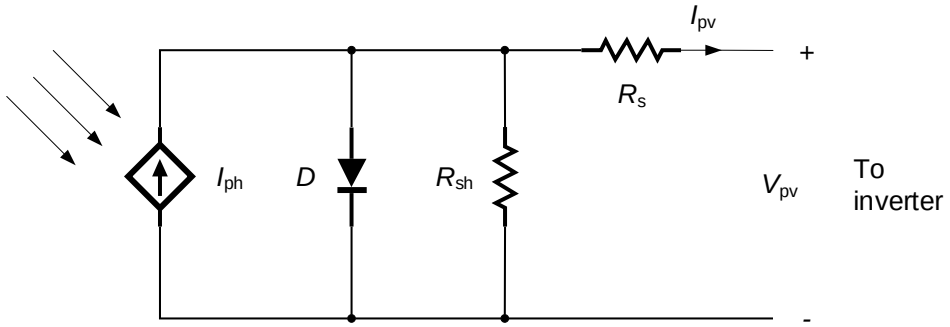


Figure 5. Model of Individual PV Cell Constituting the Studied Solar Panel

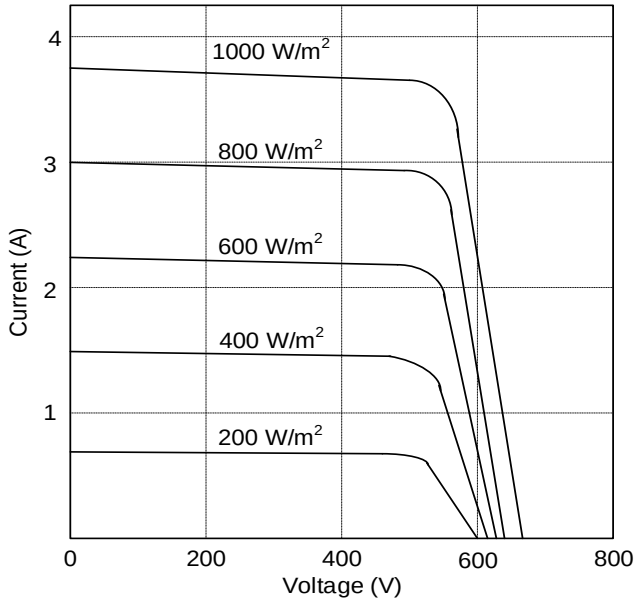


Figure 6. I-V Characteristic of Individual PV Cell at Different Solar Irradiance Levels

3.2 SPWM Inverter Design

The components used in the design of SPWM inverter is listed in Table 1. Referring to circuit topology shown in Figure 1, switch pair S_1 and S_2 is not allowed to be in the same state as pair S_3 and S_4 at a specific time. In other words, S_1 and S_2 should be on whenever S_3 and S_4 are off, and vice versa. To realize this scheme, inverting amplifier is needed. The component used for this purpose is LM741.

Table 1. The Components Utilized in SPWM Inverter Design

Component	Type/Size
IGBT	GT80J101
Flyback Diode	BYT261PIV-400
Op-Amp	LM741
R_{filter}	0.8 Ω
C_{filter}	1.5 mF

The switches are realized by using IGBT. IGBT has relatively higher voltage capability (as compared with MOSFET), with acceptable switching speed capability. GT80J101 IGBT was used, with maximum collector-to-emitter voltage V_{CE} of 600 V, maximum continuous collector current I_C of 80 A, and maximum gate-to-emitter voltage V_{GE} of 20 V. The gate driver circuit to control the IGBT operation is shown in Figure 7, where the 1N4004 diode has peak inverse voltage of 400 V. Figure 8 shows the circuit for generating SPWM signal, which will be the input for gate circuit shown in Figure 7.

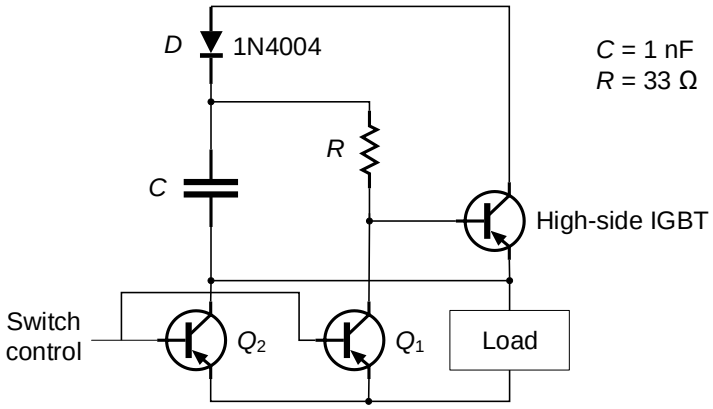


Figure 7. IGBT drive circuit

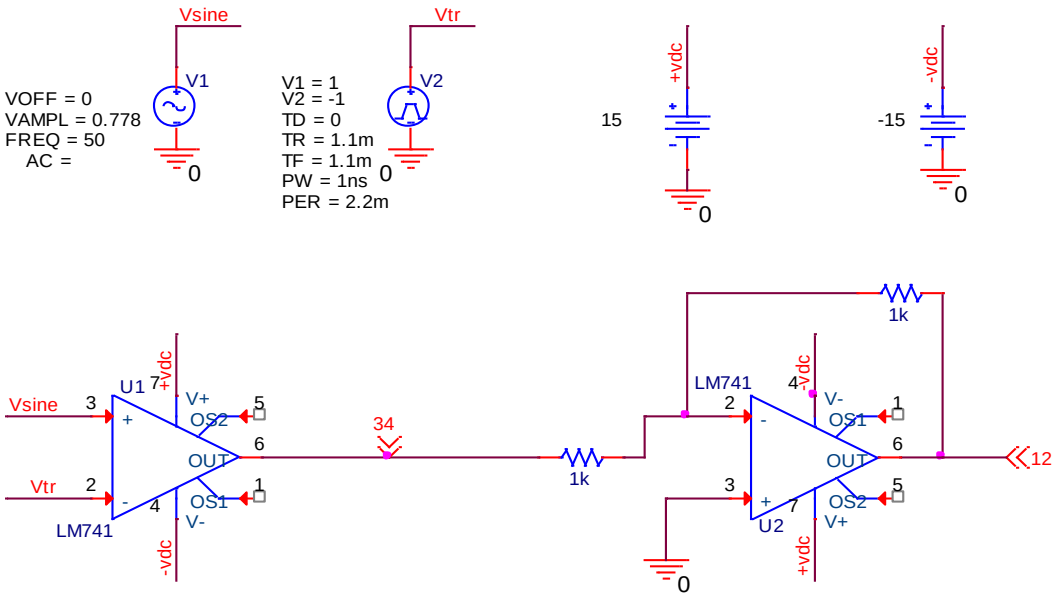


Figure 8. Implementation of SPWM-Generating Circuit

To minimize inverter output THD, passive filter was employed in this study and was realized using *RC* filter. The values of *R* and *C* are determined by using Equation 4, with Z_L = 5.24 Ω and cut-off frequency f_c = 50 Hz.

3.3 Multilevel Inverter Design

The multilevel inverter topology used is the diode-clamped (as shown in Figure 3) with 5-level output voltage. 5-level output voltage requires two DC sources. This is achieved by using two-arm capacitive voltage divider, which divides singe input DC voltage (400 V in this study) into two parts. Table 2 lists the components used in the design of multilevel inverter in this study.

Table 2. The Components Utilized in Multilevel Inverter Design

Component	Type/Size
IGBT	GT80J101
Flyback Diode	BYT261PIV-400
Diode	1N4004
Capacitor	1 nF

Modulation index was calculated by using Equation 5, while the optimal values of α_1 and α_2 were numerically sought by using Newton-Raphson technique [11].

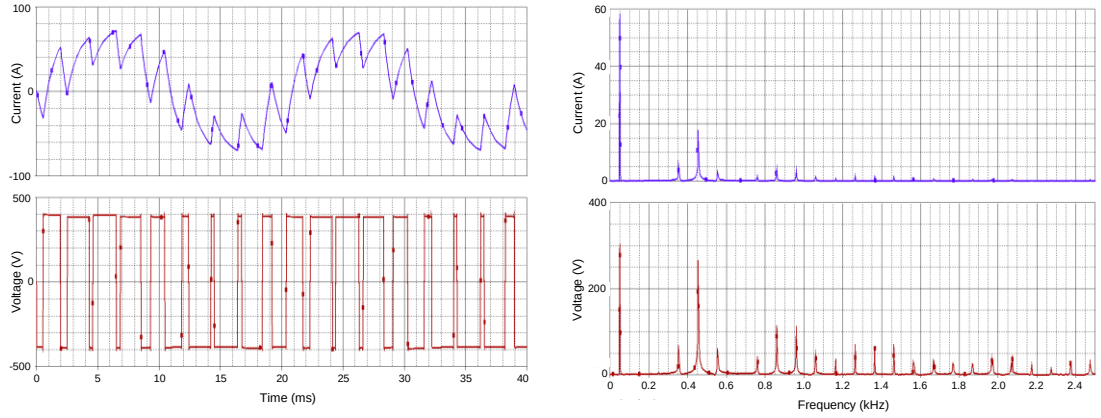
4. Results and Discussion

In this section, the performances of both inverter designed in previous section at various schemes are discussed and compared. The performance was measured in terms of output voltage and current THD.

4.1 The Performance of SPWM Inverter

For SPWM inverter, the performance was evaluated at a large number of m_f values. By such an enumeration technique, it was found that using adjacent values did not give too different THD values on inverter output. Therefore, the performance evaluation is presented here at two m_f values only, i.e. 9 and 77. At these values, simulation showed significant difference in inverter output THD.

In the first simulation, m_f value of 9 was utilized with varied input voltage. Inverter's input side was assigned voltage values in accordance with the output voltage of solar panel whose level is influenced by solar irradiance F_S. Figure 9 shows the result (output current and voltage in time and frequency domains) with F_S = 1000 W/m^2. At this solar irradiance level, the inverter input voltage became 400 V, which is desired for the design in this study.



(a) Waveforms (b) FFT spectrums

Figure 9. SPWM Inverter Current and Voltage Output with m_f = 9 and F_S = 1000 W/m^2

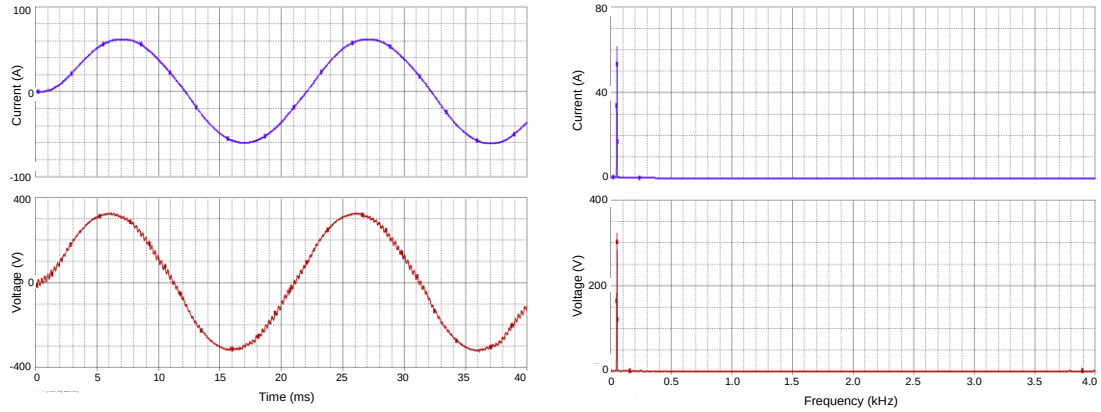
FFT representation of inverter output is given in Figure 9 (b). The fundamental components of output current and voltage are 62 A and 311 V, respectively. It was noted that this value was achieved with an amplitude modulation ratio m_a of 0.778.

The observed THD values for SPWM inverter with m_f = 9 and F_S = 1000 W/m^2 were 43% for current and 168% for voltage. To investigate the effect of level change of solar irradiance on inverter output quality, several values of solar irradiance were simulated. It was found that THD value was not a function of solar irradiance level, as indicated in Table 3. The solar irradiance level, instead, affects the fundamental component of inverter output voltage V_1.

Table 3. SPWM Inverter Output THD at Various Solar Irradiance Levels with m_f = 9

Solar Irradiance (W/m^2)	Voltage THD (%)	Current THD (%)	V_1 (V)
1000	168	43	311
800	168	43	300
600	168	43	270
400	168	43	255
200	168	43	240

THD data presented in Table 3 implies that m_f = 9 did not give high-quality inverter output, even the output is very bad, according to THD requirement specified by IEEE. Our experiment has shown that low THD was achieved at high m_f with inclusion of *RC* filter. Figure 10 shows the result with m_f = 77 and inclusion of *RC* filter. Almost-pure sinusoidal waveform in Figure 10 (a) can confirm the right choice of frequency modulation index, i.e. 77. It is further supported by FFT spectrums in Figure 10 (b). However, it was noted that relying on high m_f value only is not enough to get low voltage THD, although it worked significantly for reducing current THD. Table 4 presents THD values at several schemes used in this study.



(a) Waveforms (b) FFT spectrums

Figure 10. SPWM Inverter Current and Voltage Output with m_f = 77 and F_S = 1000 W/m^2

Table 4. THD Comparison at Two m_f Values

m_f	Voltage THD (%)	Current THD (%)
9	168	43
77	168	8
77 (with *RC* filter)	4.2	1.7

4.2. The Performance of Multilevel Inverter

THD evaluation was carried out on multilevel inverter after performing several harmonic elimination schemes. Similar to those in SPWM inverter, solar irradiance level was also taken into consideration. However, there is no inclusion of filter because we want to maximize the advantage of multilevel inverter that basically does not require filter.

Using Newton-Raphson numerical iteration technique to eliminate 3rd order harmonic and its multiples by simultaneously solving Equations 6 and 7, we obtained $\alpha_1 = 15.2^0$ and $\alpha_2 = 75.2^0$. Figure 11 shows the time-domain output waveforms and their respective FFT spectrums. It can visually be observed that 5-level inverter with such delay angles produces much better outputs as compared to those of SPWM inverter without filter inclusion shown in Figure 9.

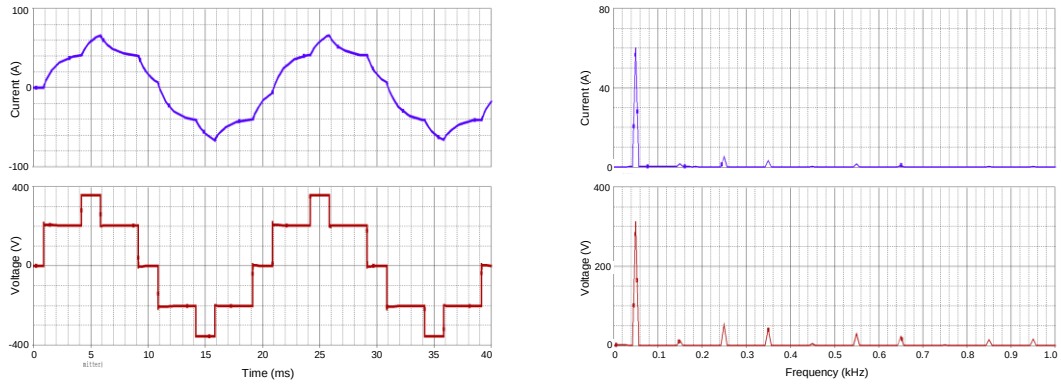
With the elimination of 3rd order harmonic and its multiples, the calculated THD values are 27% and 11% for voltage and current, respectively. These values applied for all level of solar irradiance, as listed in Table 5. Similar to those in SPWM inverter, the variation of solar irradiance level only affects the fundamental component of the output voltage V_1.

In addition to 3rd order harmonic and its multiples elimination, another harmonic order elimination was also attempted. 5th order harmonic and its multiples elimination with Newton-

Raphson iteration technique resulted in the values of 32^0 and 68^0 for α_1 and α_2, respectively. The obtained current and voltage waveforms and their associated FFT spectrums are presented in

Figure 12. The THD values for output current and voltage are 20% and 32%, respectively. These values were not affected by solar irradiance level. As in previous cases, solar irradiance level only determines the fundamental component of the output. This finding is presented Table 6**.**

Table 7 shows the recapitulation of voltage and current THD with 3rd and 5th order harmonics elimination. The effect of solar irradiance level is not presented again because it does not affect the THD. As can be seen, 3rd harmonic elimination scheme provides better results, i.e. lower voltage and current THD. The reason is that, when 3rd order harmonic elimination was performed, the number of its multiples which were also eliminated is higher than those when 5th order harmonic elimination was performed. In the first scheme, 3rd, 9th, 15th, 21st, 27th, and 33rd order harmonics were eliminated, while only 5th, 15th, 25th, and 35th order harmonics were eliminated in the second scheme.



(a) Waveforms (b) FFT spectrums

Figure 11. Multilevel Inverter Output Current and Voltage with $\alpha_1 = 15.2^0$, $\alpha_2 = 75.2^0$, and F_S = 1000 W/m²

Table 5. Multilevel Inverter Output THD at Various Solar Irradiance Levels with $\alpha_1 = 15.2^0$ and $\alpha_2 = 75.2^0$

Solar Irradiance (W/m²)	Voltage THD (%)	Current THD (%)	V_1 (V)
1000	27	11	311
800	27	11	300
600	27	11	294
400	27	11	270
200	27	11	265

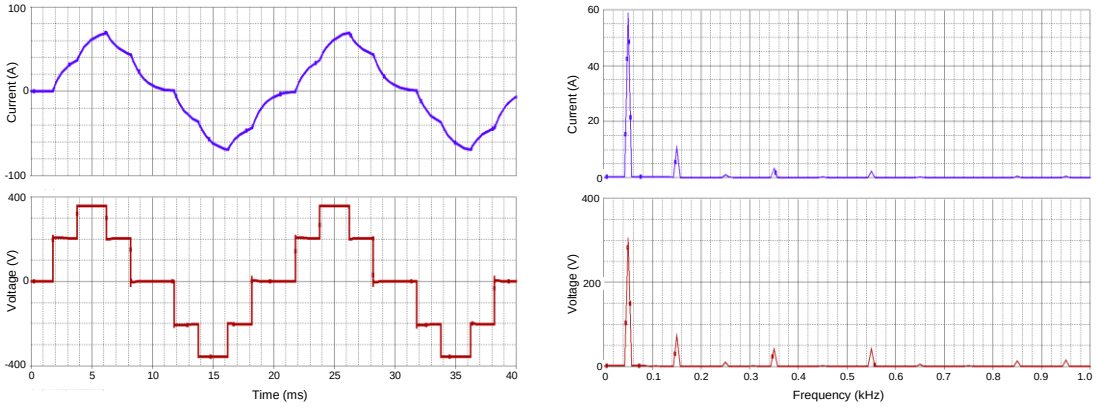
Table 6. Multilevel Inverter Output THD at Various Solar Irradiance Levels with $\alpha_1 = 32^0$ and $\alpha_2 = 68^0$

Solar Irradiance (W/m²)	Voltage THD (%)	Current THD (%)	V_1 (V)
1000	32	20	311
800	32	20	300
600	32	20	294
400	32	20	270
200	32	20	265

Table 7. Relationship between Eliminated Harmonic Orders and THD Values at Designed Multilevel Inverter

Harmonic orders eliminated	Current THD (%)	Voltage THD (%)
3, 9, 15, 21, 27, 33	11	27
5, 15, 25, 35	20	32

Figure 12. Multilevel Inverter Output Current and Voltage with $\alpha_1 = 32^0$, $\alpha_2 = 68^0$, and $F_S = 1000$ W/m^2



(a) Waveforms (b) FFT spectrums

4.3. Performance Comparison

After performing several schemes to obtain the most appropriate design for each inverter, the best scheme from each inverter design was determined and thus can easily be compared each other. The head-to-head comparison is presented in Table 8**.**

From the finding shown in Table 8, it can be said that SPWM inverter with *RC* filter performs better than 5-level inverter in terms of output current and voltage THD. Referring to IEEE 512-1992 Standard, SPWM inverter with *RC* filter can fulfill the THD requirement, i.e. 5%. In order to enhance the performance of 5-level inverter, the most possible scheme is to increase the number of level which consequently increases the complexity of inverter circuit topology.

Table 8. THD Comparison between the Designed SPWM and 5-Level Inverters

Inverter	Voltage THD	Current THD	Scheme
SPWM inverter	4.2%	1.7%	$m_f = 77$, $m_a = 0.778$, filter included
5-level inverter	27%	11%	$\alpha_1 = 15.2^0$, $\alpha_2 = 75.2^0$, no filter

5. Conclusion

The THD investigation has been carried out on SPWM inverter and 5-level inverter connected to solar panel through simulation studies. The inductive load for both inverter design has a resistance of 0.8 Ω and an inductance of 5 mH. The results can be concluded in the following statements.

1. For SPWM inverter, the optimal design was obtained by assigning amplitude modulation ratio of 0.778 and frequency modulation ratio of 77 and *RC* filter with R = 0.8 Ω and C = 1.5 mF. The THD values for this design are 1.7% and 4.2% for current and voltage, respectively.
2. For 5-level inverter, the optimal design was obtained with 3rd order harmonic elimination resulting in $\alpha_1 = 15.2^0$ and $\alpha_2 = 75.2^0$. The THD values for this design are 11% and 27% for current and voltage, respectively.
3. In terms of THD, the designed SPWM inverter has fulfilled the requirement set by IEEE 512-1992, i.e. 5%, while the designed 5-level inverter has not fulfilled yet.
4. For the above reason, the designed SPWM inverter is more suitable and more realistic to be implemented in energy system with a single solar panel as the source.

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