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Comparison between power dissipation and propagation delay on 6T SRAM cell design using GDI logic with transmission gate VMSA and voltage divider

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Abstract

The rapid evolution of the semiconductor industry has witnessed shrinking portable and mobile devices alongside an increasing demand for extended battery life. Addressing the critical challenges of speed and battery life in digital devices, this paper investigated the effectiveness of innovative low-power design techniques. Focusing on the Gate Diffusion Input (GDI) approach, a recent advancement in the field, a comprehensive analysis revealed its significant potential for reducing power consumption in digital circuits. Additionally, a comparative analysis was conducted to evaluate the performance of conventional 6T GDI SRAM cells and their Modified 6T GDI SRAM with Voltage Divider, considering the influence of Sense Amplifiers. Simulation data demonstrated that Modified 6T SRAM designs, particularly the Voltage Divider and TGVMSA variants, achieved significantly lower power dissipation and delay despite having a larger cell area. Remarkably, the proposed design substantially improved power dissipation and propagation delay, achieving $1.3\mathrm{e}^{-011}$ps, and 889.41mV at 1.8V shows that the suggested design enhances power dissipation and propagation delay. These findings suggest that the proposed design offers a promising strategy for enhancing power efficiency and performance in digital devices, thereby mitigating the limitations of battery life and speed in the modern technological landscape.

1. Introduction

The explosive growth of mobile devices and internet accessibility has fueled the demand for efficient multimedia systems. These systems prioritize extended battery life, but they face challenges from increased handling, high-resolution displays, and demanding computational tasks. Embedded static random-access memory (SRAM) plays a crucial role, consuming roughly 30% of the total power. SRAM is essential in low-power VLSI devices for high-quality applications. Among many embedded memory technologies, SRAM is uniquely positioned to deliver maximum performance while maintaining low standby power consumption [1]. Minimizing power consumption keeps your device charged. One of the main drivers of CMOS technology is the need for devices that consume little or no power. As a result, CMOS devices have low power consumption. However, it is difficult to understand that CMOS devices are less potent than devices of different technologies to reduce the need for system hardware[1]. Low-power techniques have become essential to the VLSI spectrum, especially for high-speed systems [1]. Reducing voltage offers significant power savings, as dynamic power consumption scales linearly with voltage. Nevertheless, low-voltage operation raises concerns about maintaining SRAM stability and performance.

This motivates the exploration of innovative SRAM designs for efficient multimedia applications in mobile devices [2]. Power dissipation reigns supreme as a critical design constraint in the ever-shrinking landscape of integrated circuits. Traditional circuit architectures often fall victim to excessive power wastage, hindering the efficiency and performance gains promised by VLSI technology [3]. To combat this pervasive challenge, Gate Diffusion Input (GDI) techniques and optimized sense amplifiers have emerged as promising solutions [4]. Their inherent potential to minimize power dissipation has attracted significant research interest and paved the way for their implementation in various VLSI architectures [5]. The GDI technique reduces the number of transistors in logic design, affecting the devices' size. It reduces the size of digital devices and reduces the power dissipation. This makes it ideal for designing fast, low-power circuits, as it reduces the number of transistors required, improves power characteristics, and creates new circuit topologies [6].

In handheld devices such as smartphones, SRAM is also used for power management. This is also related to battery life, a primary constraint in mobile devices [7]. One of the issues in electronic design is Power dissipation, which

comprises static and dynamic dissipation and is crucial to determining battery life. Static power dissipation occurs even when the system is in standby mode, while dynamic power dissipation is consumed during read-and-write operations in SRAM [8]. The power consumed is the product of the current and voltage drawn from the source [9]. Mobile devices require designs with low power dissipation. Dynamic power dissipation decreases with technology scaling, but static power dissipation increases in the deep submicron region [10].

Designing 6T SRAM for nanometer technology is a new challenge due to the threshold voltage variations, affecting the stability and read/write process [11]. Transistor scaling is an effective method for reducing leakage currents, but it also requires a reduction in the supply voltage to maintain power consumption. The more minor voltage differences between a transistor's drain, source, and body reduce the leakage, and the GDI (Gate Diffusion Input) is used in this paper to design SRAM cells [12]. GDI cells (Gate Diffusion Input cells) have three inputs: G (standard gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). GDI cells can design low-power circuits with low logic complexity [13]. Another critical concern for low-power design is voltage. In this paper, we operate the entire circuit at a power supply of 1.8 V using dynamic threshold logic (DTL). DTL exploits the fact that the threshold voltage of a MOSFET can be reduced by applying a voltage to the body terminal. In DTMOS (Dynamic Threshold MOSFET), the gate and body terminals are shorted through a resistive network, which acts as a voltage divider [14].

Gate diffusion input (GDI) logic is a low-power alternative to static CMOS logic. The critical difference between GDI and CMOS is that GDI does not require dedicated power and ground rails for the pMOS and nMOS transistors. Instead, it uses a single power rail and a single ground rail for both transistors. This allows GDI to implement a wide range of complex logic functions using only two transistors. One of the main advantages of GDI logic is its power efficiency. The reduced number of transistors and the elimination of dedicated power and ground rails lead to significant power savings. Additionally, GDI circuits are more flexible than CMOS circuits, making them easier to design and implement. However, GDI logic has its drawbacks. One of the main challenges is performance variation. This is because GDI circuits rely on the threshold voltage of the transistors to determine the output logic. The threshold voltage can vary depending on the process technology, the operating conditions, and the aging of the transistors. This can lead to performance variation in GDI circuits [15].

Some of the studies related to this research that propose various methods for building SRAM cells include the following research [16], which proposed a 6T SRAM cell to use sense and precharge amplifiers. The sense amplifier reads the data stored in the cell, and the precharge amplifier sets the initial state of the cell before a read or write operation. Overall, the power consumption of an SRAM cell with sense and precharge amplifiers will depend on various factors, including the specific design of the cell and the operating conditions. The proposed method achieved an access time of less than 2.5ns using 0.55nm technology with an operating voltage of 1.8v. Research [17] proposed 8T SRAM and the sense amplifier and analyzed the delay and power measurement on transmission gate voltage mode sense amplifier and voltage mode sense amplifier. The design of TGVMSA using 1.5v/45nm CMOS technology has a higher cell area but lower power dissipation and delay. The result minimizes the power dissipation and propagation delay compared to the voltage mode sense amplifier. Research [14] proposed that a power 16X16 SRAM array is designed to store 256 bits. A power consumption of 101.6 uW and 25MHz operating frequency is achieved using 180nm technology.

In response to the power-intensive needs of mobile multimedia, this research proposes an innovative 6T SRAM design tailored for nanometer technology. By utilizing Gate Diffusion Input (GDI), adding a voltage divider, and selecting a good sense amplifier, our design effectively mitigates power dissipation, solving the challenges of battery longevity and performance constraints under low voltages. By optimizing the transistor count and harnessing body biasing methods, we aim to establish a highly efficient data storage solution suited for mobile devices with limited resources.

2. Research Method

2.1 Schematic of 6T SRAM GDI Architecture

A 6-transistor SRAM cell (6T GDI SRAM cell) is a simple SRAM cell that uses 4 NMOS transistors and 2 PMOS transistors, as shown in Figure 1(a). It uses a cross-coupled structure to create an inverter, which stores the bit value (Q and Q_bar) within itself [18]. The memory's bit line and bit line bar are used for read and write operations and are connected to the cell using two NMOS access transistors [19]. When the word line (WL) is asserted, the access transistors turn on, connecting the bit line and bit line bar to the cell [20]. This allows the cell to be read or written to. The bit lines are precharged to VDD during a read operation in a 6T SRAM cell [21]. When the word line is asserted, the PMOS access transistors in the selected cell turn on, connecting the bit lines to the cell's internal nodes. If the cell stores a logic 0, the bit lines will be discharged to the ground [22]. If the cell stores logic 1, the bit lines will remain at VDD. After the bit lines have been connected to the cell, a sense amplifier detects the voltage difference between the two- bit lines. If the bit lines are at different voltages, the sense amplifier amplifies the difference and produces a valid output signal. The sense amplifier will produce an invalid output signal if the bit lines are at the same voltage.

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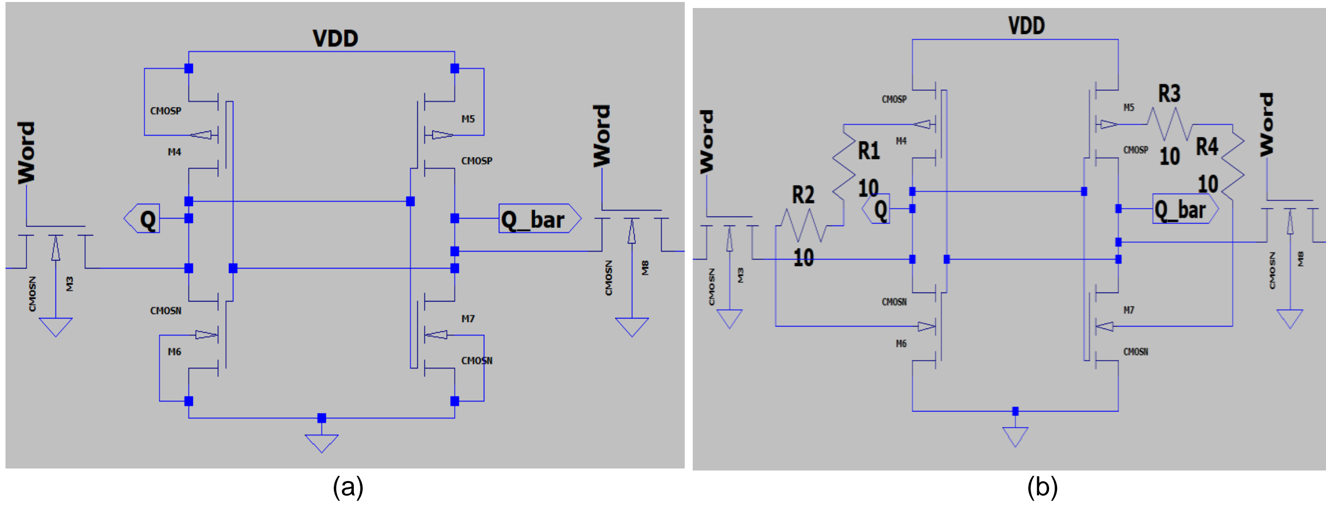


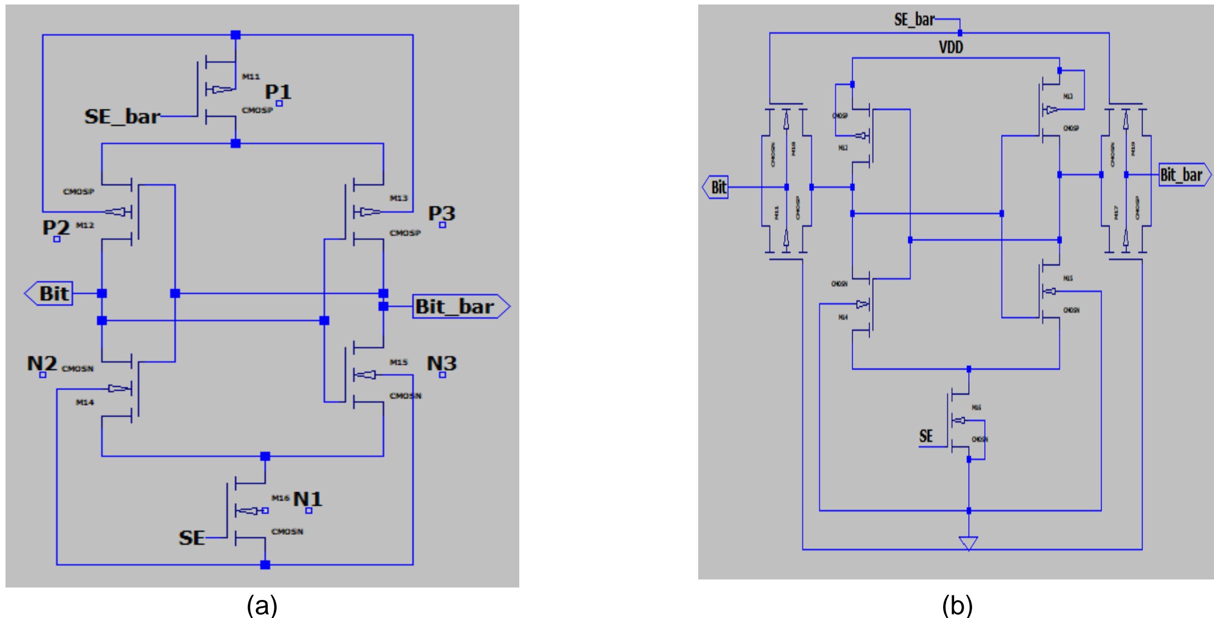
(a) (b)

Figure 1. (a) Schematic of 6T GDI SRAM (b) Schematic of Modified SRAM Voltage Divider

This research uses a GDI inverter with a voltage divider and fluctuation instead of CMOS inverters, as shown in Figure 1 (b). Better logic swing and improved data storage are two benefits of Gate Diffusion Input. The latch is connected to two complimentary bit line columns (BL and BLB) by two pass gates, and the two pass gates are activated when the word line asserts one (WL=1). The prior data in the latch remains unaltered when WL=0 because the two pass gates are isolated to the latch [23].

2.2 Schematic of Sense Amplifier

During a read cycle, the sense amplifier determines what value is stored in an SRAM cell and displays that value at the output [24]. Each column of cells in the SRAM array only needs one sense amplifier since only one row of data is accessed during each read cycle [25]. A sense amplifier determines whether a cell is storing a logic 1 or 0 by detecting a relatively slight difference between the voltages of the two-bit lines and magnifying the difference at the output. Before each read cycle, the bit lines are precharged to ensure the variation in bit line voltages is due to the value stored in the cell [26].



(a) (b)

Figure 2. (a) Schematic of Basic Latch Voltage Sense Amplifier (b) Schematic of Transmission Gate VMSA

2.3 Simulation Design

Circuit performance will be analyzed by visualizing output graphs and extracting specific parameter values via the SPICE directive commands. These commands allow precise measurement of essential parameters throughout the simulation, complementing the insights gleaned from the graphical output.

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```
.lib C:\Users\rezaa\OneDrive\Documents\LTspiceXVII\lib\cmp\standard.mos
.include tsmc018.lib
.tran 80n
* Some measurements
.param VDD =  1.8
.measure Voutmax MAX V(q)
.measure Voutmin MIN V(q)
.measure tfall ; Falling time
+TRIG V(q) VAL = '0.8*1.0' FALL=1
+TARG V(q) VAL = '0.2*1.0' FALL=1
.measure trise ; Rising time
+TRIG V(q) VAL = '0.2*1.0' RISE=1
+TARG V(q) VAL = '0.8*1.0' RISE=1
.measure tpdf ; Falling propagation delay
+TRIG V(q_bar) VAL = '0.8*1.0' RISE=1
+TARG V(q) VAL = '0.2*1.0' FALL=1
.measure tpdr ; Rising propagation delay
+TRIG V(q_bar) VAL = '0.2*1.0' FALL=1
+TARG V(q) VAL = '0.8*1.0' RISE=1
.measure tpd PARAM '{tpdf+tpdr}/2' ; Avg. propagation delay
.backanno
.end
```

Figure 2. Spice Directive Measuring Output

In Figure 2, the spice directive command, measurement values from the waveform data, including maximum and minimum values, rising and falling times, and propagation delay. The displayed data reveals a VDD parameter of 1.8, which applies to all comparisons, regardless of whether SRAM GDI or Modified SRAM is utilized. This optimal value, achieved through the outlined procedure, is a baseline for benchmarking further measurements. Figure 2 illustrates the calculations used to estimate these values, employing the tsmc018.lib library file and. tran 80n transient analysis.

Several key measurements are employed within the code to assess the circuit's performance. Voutmax captures the maximum voltage at node 'q' during the simulation, while Voutmin tracks the minimum voltage. The falling time of the signal at node 'q,' referred to as tall, measures the time required for the voltage to transition from 80% of VDD to 20% of VDD. Conversely, trise measures the rising time of the signal, indicating the time taken for the voltage to ascend from 20% to 80% of VDD. To evaluate signal propagation characteristics, pdf calculates the falling propagation delay, representing the time delay between the input signal at node 'q_bar' reaching 80% of VDD and the subsequent 80% decline in voltage at node 'q.' Conversely, trade measures the rising propagation delay, quantifying the time delay between the input signal at node 'q_bar' reaching 20% of VDD and the subsequent 80% rise in voltage at node 'q.' Lastly, tpd provides a comprehensive metric of overall signal propagation speed by averaging the falling and rising propagation delays.

3. Results

3.1 Modified 6T SRAM Voltage Divider with TGVMSA Simulation

Figure 3 presents the operational waveforms of the proposed 6T SRAM cell. The red line shows the data being written to the cell. The pink and light green lines control whether the cell is being read from or written to. The green line shows the data being read from the cell. The word line signal (not shown) allows data to flow in and out of the cell. New data is written to the cell when the write signal is high. The word line signal is used for reading and writing, so it is twice as fast as the write signal. When both word and write signals are high, the cell's output is copied back to the input.

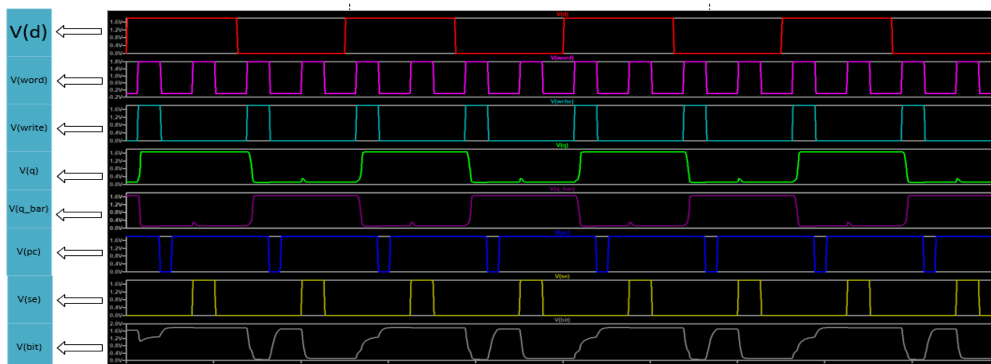

Figure 3. Output Waveform of Modified 6T SRAM Voltage Divider with TGVMSA

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Table 1. Comparison Average Output Q Power Dissipated

Power Supply	6T GDI SRAM with Basic Latch Sense Amplifier	6T SRAM GDI with TGVMSA	Modified 6T SRAM Voltage Divider with Basic Latch Sense Amplifier	Modified 6T SRAM Voltage Divider with TGVMSA
0.9 V	457.2mV	454.46mV	466.37mV	462.62mV
1.0 V	508.98mV	504.24mV	505.55mV	509.02mV
1.1 V	560.39mV	582.97mV	550.16mV	552mV
1.2 V	611.8mV	614.17mV	604.88mV	599.96mV
1.8 V	**917.2mV**	**917.45mV**	**893.31mV**	**889.41mV**

Table 1 shows the power consumption of two different SRAM designs (6T GDI and Modified 6T Voltage Divider) at different power supply voltages (0.9V to 1.8V). Both designs have two versions: one with Basic Latch Sense Amplifier and TGVMSA. Generally, higher voltages lead to higher power consumption across all configurations. The TGVMSA versions are slightly more power-efficient within each voltage level than the Basic versions. The Modified 6T Voltage Divider design is more power-efficient overall, especially at lower voltages. It consumes the least power at 0.9V and 1.1V, but the difference diminishes at higher voltages.

Table 2. Propagation Delay Comparison of Different Method SRAM at 180nm Technology

Parameter	6T GDI SRAM with Basic Latch Sense Amplifier	6T SRAM GDI with TGVMSA	Modified 6T SRAM Voltage Divider with Basic Latch Sense Amplifier	Modified 6T SRAM Voltage Divider with TGVMSA
Vout MAX	1.88	1.88	1.67	1.67
Vout Min	-0.01	-0.01	0.11	0.11
Falling Time	$9.60e^{-011}$	$1.36e^{-010}$	$1.03e^{-008}$	$1.29e^{-010}$
Rising Time	$-1.50e^{-008}$	$-1.50e^{-008}$	$-1.45e^{-008}$	$1.80e^{-010}$
Falling Propagation Delay	$1.03e^{-008}$	$1.04e^{-008}$	$1.04e^{-008}$	$7.03e^{-011}$
Rising Propagation Delay	$-1.96e^{-010}$	$-2.34e^{-010}$	$-3.24e^{-010}$	$-4.50e^{-011}$
Propagation Delay	$5.08e^{-009}$ps	$5.13e^{-009}$ps	$5.03e^{-009}$ps	$1.27e^{-011}$ps

Table 2 shows a new circuit called the Modified 6T SRAM Voltage Divider with TGVMSA significantly improves voltage range and speed compared to the other designs. It can handle a broader range of voltages, making it less noise-sensitive and more accurate. It is also much faster, making it ideal for high-performance applications where speed is critical. Overall, the Modified 6T SRAM Voltage Divider with TGVMSA significantly improved over previous designs, making it a promising candidate for future applications.

Table 3. Technology Propagation Delay Comparison of Different Method SRAM Technology with another Research.

Parameter	8T SRAM with VMSA at 1.5V (µs) (Chandra Kishore et al.,2019)	8T SRAM with TGVMSA at 1.5V (µs) (Chandra Kishore et al.,2019)	6T Standard GDI SRAM with TGVMSA (This Research)	Modified 6T SRAM Voltage Divider with TGVMSA (This Research)
Propagation Delay	1364,22 µs	1028,76 µs	$5.03e^{-009}$ps	$1.27e^{-011}$ps

Table 3 compares the propagation delay in different types of SRAM memory designs. The propagation delay for the 8T SRAM with VMSA stands at 1364,22 µs, while the 8T SRAM with TGVMSA has a lower delay at 1028,76 µs. On

the other hand, the newer designs, specifically the 6T Standard GDI SRAM with TGVMSA and the Modified 6T SRAM Voltage Divider with TGVMSA, demonstrate significantly reduced delays at 5.03e^{-009}ps and 1.27e^{-011}ps, respectively. This indicates a substantial advancement in reducing delay times with the newer SRAM designs compared to the earlier 8T configurations.

Table 4. Power Consumption Comparison of Different Method SRAM Technology with another Research.

Parameter	6T Standard GDI SRAM with Basic Latch Sense Amplifier (This Research)	6T Standard GDI SRAM with TGVMSA (This Research)	Modified 6T SRAM Voltage Divider with Basic Latch Sense Amplifier (This Research)	Modified 6T SRAM Voltage Divider with TGVMSA (This Research)	Kumar et al., 2017
Power Consumption	62.504 µW	80.594 µW	61.809 mW	61.817 mW	101.6 µW

Table 4 shows the comparison results between this method and the other methods. While our newly proposed Modified 6T SRAM Voltage Divider exhibits impressive speed with TGVMSA (1.27 ps propagation delay), its power consumption (61.817 mW) remains comparable to its Basic Latch Sense Amplifier counterpart (61.809 mW). While this indicates minimal power overhead for the speed improvement, both designs still surpass Kumar et al.'s 2017 work (101.6 µW) by nearly 40%. Further optimization efforts are warranted to address the power consumption disparity between Basic Latch Sense Amplifier and TGVMSA variants within the Modified 6T SRAM Voltage Divider architecture, enabling a genuinely balanced solution for high-performance, low-power SRAM design.

4. Conclusion

The current work suggests creating a 6T SRAM using the Gate Diffusion Input (GDI) and TGVMSA schemes, shown through simulation, to incinerate low power dissipation and propagation delay. It is pointed out that the sense amplifier reaction time depends on bit line differential voltage. Compared to the 6T GDI SRAM used in the design, it is shown that Modified 6T SRAM with TGVMSA delivers less delay and less rising and falling time, improving cell stability. The proposed circuit scheme (Voltage Divider and TGVMSA) offers an improvement in delay reduction with results of 1.27 $e^{-011}ps$ at 1.8V and 889.41mV at 1.8V process corners at the expense of power dissipation of the SRAM cell when compared to the GDI technique, according to the results of the comparison. The analysis is obtained by comparing this study's output voltage value with the previous research used as a reference. In this study, a 6T SRAM circuit has been modified so that the propagation delay and power consumption are minor; then, the circuit design will be implemented in 180nm CMOS technology. The propagation delay values for the 8T SRAM with VMSA and TGVMSA at 1.5V, as reported by Chandra Kishore et al., demonstrate a noticeable difference, with the TGVMSA configuration exhibiting a lower delay (1028.76 µs) compared to the VMSA (1364.22 µs). However, the focus of interest lies in the novel 6T SRAM configurations presented in this research.

The 6T Standard GDI SRAM with TGVMSA showcases an exceptionally reduced propagation delay of 5.03e^{-009} ps, while the Modified 6T SRAM Voltage Divider with TGVMSA exhibits an even more remarkable delay of 1.27 e^{-011} ps. In the 6T Standard GDI SRAM with TGVMSA, there was a noticeable increase in power usage, recorded at 80.594 µW. However, the genuine interest lies in the modified 6T SRAM configurations. The Modified 6T SRAM Voltage Divider with Basic Latch Sense Amplifier indicated a substantial spike in power consumption, reaching 61.809 mW. The Modified 6T SRAM Voltage Divider with TGVMSA showcased a similar power consumption level, measured closely at 61.817 mW. This comparison against Kumar et al. findings, with a power consumption of 101.6 µW, illustrates the significance of advancements in this research in achieving lower power utilization, especially in the modified 6T configurations. Optimizing future research efforts in SRAM cell design can yield significant performance improvements. Two key areas warrant further exploration: size reduction and improved sense amplifier design. First, scaling down the existing schematic designs enhances packing density and potentially reduces power consumption and operational voltage. Second, research into enhanced sense amplifier designs holds immense potential. Developing high-gain, low-power, and noise-resilient sense amplifiers is crucial for reliable and accurate data retrieval from increasingly miniaturized SRAM cells.

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